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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/148,606	09/04/1998	KIYOSHI YONEDA	5586D-6885	3618

26021 7590 05/08/2002

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EXAMINER	
ZAMANI, ALI A	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/148,606	Yoneda et al.
Examiner	**Art Unit**
Ali Zamani	2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 13, 2002*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-22* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-22* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *18*

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

The indicated allowability of claims 9, 14, 17-18 and 20-22 are withdrawn in view of the newly discovered reference (s) to . Rejections based on the newly cited reference (Kato et al. and Kousai et al.) follow.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. (US Pat. No. 5,789,763).

3. In regard to claims 1-4 , Kato et al. teach A semiconductor device in which a plurality of semiconductor elements are formed on a substrate, wherein in some or all of said semiconductor elements, a channel width of a channel region formed in a semiconductor layer to which laser annealing is applied is larger than a channel length thereof. Kato et al. also teach on a substrate on which TFTs for driving pixels which are composed of polycrystalline semiconductor, there are further driving circuits including TFTs which are composed of polycrystalline semiconductors and by using a method of arranging the TFTs for row driving circuits or column driving circuits on extension lines of the TFTs for displaying pixels and the TFTs for either one

of the row driving circuits and the column driving circuits can be simultaneously beam-annealed to form polycrystalline layers (col. 3, lines 26-42). Kato et al. further teach when the TFTs having a longer Channel width are provided, the column-driver-TFT is divided into plural TFTs to drive in parallel which the TFTs can be disposed in pitch gaps in the direction of column electrode line. Kato et al. further teach the annealing can be conducted at a pitch of 1/M (M is an integer) of the pitch of the pixels in the direction of row electrode line and the pitch can be changed during the annealing, accordingly the number of times of beam-anneal-scanning is equal to the number of the straight lines. However, the pinch may not be constant and the distance between specified adjacent two straight lines and the arrangement of a constant pinch further contributes improvement in the throughput and stability and it is necessary to arrange the circuits on the spright lines (beam-anneal-scanning lines to form the stripes) having a substantially the same width as that of the beam spot since the beam-anneal-scanning is effected by the laser beam (see col. 9, lines 1-31). Thus, it would have been obvious to one of ordinary skill in the art by changing the channel width size " see IN Re Rose 105 USPQ 237 (CCPA 1955)" and repositioning of the direction "see In Re Japikse 86 USPQ 70 (CCPA 1950)" to provide a method relates to a semiconductor device having a plurality of semiconductor elements on a substrate, wherein some or all of the semiconductor elements have a plurality of channel areas which are formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas are electrically connected in neither vertical nor parallel to each other and arranged separately and/or arranged in different direction to each other.

4. Claim 5- 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kousai et al. (US Pat. No. 5,744,824).

5. In regard to claims 5-22, Kousai et al. teach a display device, comprising: a plurality of pixel electrodes arranged on a substrate; a plurality of first thin-film transistors connected to corresponding pixel electrodes among plurality of pixel electrodes for supplying signals for operating pixels to the connected pixel electrodes; and a plurality of second thin-film transistors constituting a scanning drive circuit for scanning plurality of first thin-film transistors and/or a display drive circuit for supplying display signals to plurality of first thin-film transistors (see col. 4, lines 1-35) wherein in some or all of plurality of second thin-film transistors, a channel width of a channel region formed in a semiconductor film to which laser annealing is applied (col. 6, lines 30-45). Kousai et al. also teach a method for producing a semiconductor device including a first thin film transistor having a first channel layer formed of a first crystalline silicon layer and a second thin film transistor having a second channel layer formed of a second crystalline silicon layer includes the steps of forming an amorphous silicon layer having a selected area including a catalytic element introduced thereto for crystal growth on a substrate having an insulation surface; performing first annealing to generate a crystal nucleus in the selected area of the amorphous silicon layer, thereby crystalllizing the selected area, and consecutively causing crystal growth to proceed in a lateral direction form the selected area to form the second crystalline silicon layer; and performing second annealing to crystallize the rest of the amorphous silicon layer which remains in an amorphous state after the first annealing, thereby forming the

first crystalline silicon layer. Kousai et al. further teach that only a selected area of an amorphous silicon layer which is first crystallized into a crystalline silicon layer using a catalytic element such as nickel is used to form a TFT for a peripheral driving circuit and by such a method, a TFT for a peripheral driving circuit can be formed of a crystalline silicon layer having a substantially uniform crystal growth direction and a very low density of crystal defects (dislocations) and the TFT formed of such a later has a very high mobility and prevents excessive increase of the "OFF" current. Since the crystal growth direction of area to which a catalyst is introduced can be adjusted by the pattern of the mask, any structure of TFT can be configured easily for a peripheral driving circuit (col. 12, lines 28-50). Thus, it would have been obvious to one of ordinary skill in the art to the art by changing the channel width size " see IN Re Rose 105 USPQ 237 (CCPA 1955)" and repositioning of the direction "see In Re Japikse 86 USPQ 70 (CCPA 1950)" to provide a method relates to a semiconductor device having a in some or all of plurality of second thin-film transistors, by changing the channel width being larger than a channel length, and a channel direction of some or all of second thin-film transistors being formed non-parallel with and non-orthogonal to a channel width direction of first thin-film transistors.

6. prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Koga et al., Yamazaki et al. are made of record to show various type of semiconductor devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ali Zamani whose telephone number is (703) 308-6414. The examiner can normally be reached on Monday through Friday from 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerepe, can be reached on (703) 305-4709.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washingto, DC 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Ali Zamani

May 6, 2002

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600